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EXAMINER	
CHENG, PETER L	

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2625	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

mailroom@bskb.com

Office Action Summary	Application No.	Applicant(s)
	10/623,645	WANG ET AL.
	Examiner	Art Unit
	PETER L. CHENG	2625

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _11 June 2009_.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) _2 and 5-15_ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) _2 and 5-15_ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _7/22/2003 and 2/6/2008_ is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____.

DETAILED ACTION

1. It has been noted that **claim 2** has been amended to overcome the rejection made in the previous office action. However, it is also noted that **claim 2** has been amended so that it now claims a *different embodiment*; this *different embodiment* corresponds to the *embodiment cited in the originally-filed claim 4*. It is further noted that claim 4 was cancelled in Applicants' reply of **2/6/2008**.

2. It has been noted that newly-added **claim 6** corresponds to the *embodiment cited in the originally-filed claim 1*. *The claims differ in that the current limitation, a "sequence of time slots", was originally referred to as a "sequence of the primary colors".* It is further noted that claim 1 was cancelled in Applicants' reply of **11/18/2008**.

3. It has been noted that newly-added **claim 8** corresponds to the *embodiment cited in the originally-filed claim 2* which *was rejected in the previous office action*. *The claims differ in that the current limitation, a "sequence of time slots", was originally referred to as a "sequence of the primary colors".*

4. It has been noted that newly-added **claim 11** corresponds to the *embodiment cited in the originally-filed claim 3*. *The claims differ in that the current limitation, a "sequence of time slots", was originally referred to as a "sequence of the primary colors".* It is further noted that claim 3 was cancelled in Applicants' reply of **2/6/2008**.

Drawings

5. The drawings are objected to because:

- **Fig. 3 (**as filed on **2/6/2008): per page 6, lines 10 – 12 (**of the originally-filed disclosure**)**, for clarity, suggest adding a "third line" connecting "data bus" **6** to the "sample and hold register" **2** to emphasize the data size relation between the "DACs" **3a**, **3b** and **3c** and the "sample and hold register" **2**;

- **Fig. 4 (**as originally-filed**):** per **page 7, lines 4 – 7 (**of the originally-filed disclosure**)**, the interface between the "shift register" **1** and the "sample and hold register" **2** should be the same as the corresponding interface shown in **Fig. 3**; **Fig. 4** currently illustrates a single line connecting the "shift register" **1** and the "sample and hold register" **2**; *as with the suggestion made for **Fig. 3** above, suggest that three lines should connect the "shift register" **1** and the "sample and hold register" **2**;*

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an

amended drawing should not be labeled as “amended.” If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either “Replacement Sheet” or “New Sheet” pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

6. The disclosure is objected to because of the following informalities:

- **Page 2 (***of the originally-filed disclosure***), lines 11 - 12:** the specification states “*a <u>shift register receiving image data</u> of three primary colors in serial and <u>outputting the image data</u> of the three primary colors in parallel*”; however, the “image data” **6** of **Fig. 3** is not “received and outputted” by the “shift register” **1** (**Fig. 3**); a “shift register” typically provides a “shifted pulse signal” which is used by the “sample and hold register” to capture digital data from a “data bus”; *suggest re-writing this portion of the specification to more*

clearly define the relation between the "shift register" and the "sample and hold register";

- **Page 3 (***of the originally-filed disclosure***), lines 3 - 6:** the specification states "*a shift register receiving image data of three primary colors in serial and outputting the image data of the three primary colors in parallel*"; however, the "image data" **6** of **Fig. 4** is not "received and outputted" by the "shift register" **1** (**Fig. 4**); a "shift register" typically provides a "shifted pulse signal" which is used by the "sample and hold register" to capture digital data from a "data bus"; *suggest re-writing this portion of the specification to more clearly define the relation between the "shift register" and the "sample and hold register*";

- **Page 3 (***of the originally-filed disclosure***), lines 26 - 28:** the specification states "*a shift register receiving and outputting image data of the three primary colors*"; however, the "image data" **6** of **Fig. 5** is not "received and outputted" by the "shift register" **8** (**Fig. 5**); a "shift register" typically provides a "shifted pulse signal" which is used by the "sample and hold register" to capture digital data from a "data bus"; *suggest re-writing this portion of the specification to more clearly define the relation between the "shift register" and the "sample and hold register*";

- **Page 4 (***of the originally-filed disclosure***), lines 14 - 16:** the specification states "*a shift register receiving and outputting image data of one of the three primary colors*"; however, the "image data" **6** of **Fig. 5** is not "received and outputted" by the "shift register" **8** (**Fig. 5**); a "shift register" typically provides a "shifted pulse signal" which is used by the "sample and hold register" to capture digital data from a "data bus"; *suggest re-writing this portion of the specification to more clearly define the relation between the "shift register" and the "sample and hold register"*;

- **Page 6 (***of the originally-filed disclosure***), lines 6 - 9:** the specification states "[the] *shift register 1 receives image data of the three primary colors in serial through a serial data bus 15 and outputs the image data of the three primary colors in parallel*"; however, the "image data" **6** of **Fig. 3** is not "received and outputted" by the "shift register" **1** (**Fig. 3**); a "shift register" typically provides a "shifted pulse signal" which is used by the "sample and hold register" to capture digital data from a "data bus"; *suggest re-writing this portion of the specification to more clearly define the relation between the "shift register" and the "sample and hold register"*;

- **Page 7 (***of the originally-filed disclosure***), lines 9 - 11:** the specification states "[the] *shift register 1 receives image data of the three primary colors in serial through the serial data bus 15 and outputs the image data of the three*

primary colors"; however, the "image data" **6** of **Fig. 4** is not "received and outputted" by the "shift register" **1** (**Fig. 4**); a "shift register" typically provides a "shifted pulse signal" which is used by the "sample and hold register" to capture digital data from a "data bus"; *suggest re-writing this portion of the specification to more clearly define the relation between the "shift register" and the "sample and hold register*";

- **Page 8 (***of the originally-filed disclosure***), lines 12 - 14:** the specification states "[the] *<u>shift register 8 receives and outputs image data</u> of the three primary colors*"; however, the "image data" **6** of **Fig. 5** is not "received and outputted" by the "shift register" **8** (**Fig. 5**); a "shift register" typically provides a "shifted pulse signal" which is used by the "sample and hold register" to capture digital data from a "data bus"; *suggest re-writing this portion of the specification to more clearly define the relation between the "shift register" and the "sample and hold register*";

Appropriate correction is required.

Claim Objections

7. Claim 2 is objected to because of the following informalities:

- **Line 7:** as noted in the corresponding objection to the specification, the “image data” **6** of **Fig. 5** is not “received and outputted” by the “shift register” **8** (**Fig. 5**); a “shift register” typically provides a “shifted pulse signal” which is used by the “sample and hold register” to capture digital data from a “data bus”;

- **Line 21:** per **claim 2, lines 17 – 18**, suggest replacing **the gamma reference voltage** with **the gamma reference voltage <u>corresponding to the one of the three primary colors</u>**;

8. Claim 6 is objected to because of the following informalities:

- **Line 2:** for clarity, suggest replacing **wherein each of scan durations of the horizontal lines** with **wherein [[~~each of~~]] <u>a</u> scan <u>duration</u> [[~~durations~~]] of <u>each of</u> the horizontal lines**;

- **Line 4:** as noted in the corresponding objection to the specification, the “image data” **6** of **Fig. 3** is not “received and outputted” by the “shift register” **1** (**Fig. 3**); a “shift register” typically provides a “shifted pulse signal” which is used by the “sample and hold register” to capture digital data from a “data bus”;

- **Lines 5 - 6:** for clarity, suggest replacing **within each of the scan durations of the horizontal lines** with **within [[~~each of the~~]] the scan duration [[~~durations~~]] of each of the horizontal lines**;

- **Line 7:** per **claim 6, line 4**, suggest replacing **the image data** with **the image data of the three primary colors**;

- **Lines 9 - 10:** for clarity, suggest replacing **within each of the scan durations of the horizontal lines** with **within [[~~each of the~~]] the scan duration [[~~durations~~]] of each of the horizontal lines**;

9. Claim 8 is objected to because of the following informalities:

- **Line 2:** for clarity, suggest replacing **wherein each of scan durations of the horizontal lines** with **wherein [[~~each of~~]] a scan duration [[~~durations~~]] of each of the horizontal lines**;

- **Line 4:** as noted in the corresponding objection to the specification, the “image data” **6** of **Fig. 4** is not “received and outputted” by the “shift register” **1** (**Fig. 4**); a “shift register” typically provides a “shifted pulse signal” which is used by the “sample and hold register” to capture digital data from a “data bus”;

- **Line 4:** suggest replacing **three primary colors** with **<u>the</u> three primary colors**;

- **Lines 5 - 6:** for clarity, suggest replacing **within each of the scan durations of the horizontal lines** with **within [[~~each of the~~]] <u>the</u> scan <u>duration</u> [[~~durations~~]] of <u>each of</u> the horizontal lines**;

- **Line 10:** per **claim 8, line 9**, suggest replacing **them** with **[[~~them~~]] <u>the image data of the three primary colors</u>**;

- **Line 11:** for clarity, suggest replacing **within each of the scan durations of the horizontal lines** with **within [[~~each of the~~]] <u>the</u> scan <u>duration</u> [[~~durations~~]] of <u>each of</u> the horizontal lines**;

- **Lines 13 - 14:** for clarity, suggest replacing **within each of the scan durations of the horizontal lines** with **within [[~~each of the~~]] <u>the</u> scan <u>duration</u> [[~~durations~~]] of <u>each of</u> the horizontal lines**;

- **Line 15:** per **claim 8, lines 9 - 10**, suggest replacing **the image data** with **the image data <u>of the three primary colors</u>**;

10. Claim 10 is objected to because of the following informalities:

- **Line 4:** suggest replacing **image data** with **<u>the</u> image data**;

11. Claim 11 is objected to because of the following informalities:

- **Line 2:** for clarity, suggest replacing **wherein each of scan durations of the horizontal lines** with **wherein [[~~each of~~]] <u>a</u> scan <u>duration</u> [[~~durations~~]] of <u>each of</u> the horizontal lines**;

- **Line 5:** as noted in the corresponding objection to the specification, the "image data" **6** of **Fig. 5** is not "received and outputted" by the "shift register" **8** (**Fig. 5**); a "shift register" typically provides a "shifted pulse signal" which is used by the "sample and hold register" to capture digital data from a "data bus";

- **Lines 6 - 7:** for clarity, suggest replacing **within each of the scan durations of the horizontal lines** with **within [[~~each of the~~]] <u>the</u> scan <u>duration</u> [[~~durations~~]] of <u>each of</u> the horizontal lines**;

- **Line 8:** per **claim 11, line 5**, suggest replacing **the image data** with **the image data <u>of the three primary colors</u>**;

- **Line 11:** per **claim 11, line 5**, suggest replacing **the image data** with **the image data <u>of the three primary colors</u>**;

12. Claim 13 is objected to because of the following informalities:

- **Line 1:** as noted in the corresponding objection to the specification, the "image data" **6** of **Fig. 5** is not "received and outputted" by the "shift register" **8** (**Fig. 5**); a "shift register" typically provides a "shifted pulse signal" which is used by the "sample and hold register" to capture digital data from a "data bus";

- **Line 1:** per **claim 11, line 5**, suggest replacing **receives outputs** with **receives <u>and</u> outputs**;

- **Line 4:** suggest replacing **image data** with **<u>the</u> image data**;

13. Claim 14 is objected to because of the following informalities:

- **Line 2:** for clarity, suggest replacing **wherein each of scan durations of the horizontal lines** with **wherein [[~~each of~~]] <u>a</u> scan <u>duration</u> [[~~durations~~]] of <u>each of</u> the horizontal lines**;

- **Lines 5 - 6:** for clarity, suggest replacing **within each of the scan durations of the horizontal lines** with **within [[~~each of the~~]] <u>the</u> scan <u>duration</u> [[~~durations~~]] of <u>each of</u> the horizontal lines**;

- **Line 8:** for clarity, suggest replacing **within each of the scan durations of the horizontal lines** with **within [[~~each of the~~]] the scan duration [[~~durations~~]] of each of the horizontal lines**;

- **Line 10:** per **claim 14, line 7**, suggest replacing **the reference voltages** with **the gamma reference voltages**;

14. Claim 15 is objected to because of the following informalities:

- **Line 9:** per **claim 15, line 4**, suggest replacing **the image data** with **the image data of the one of the three primary colors**;

- **Lines 9 - 10:** per **claim 15, lines 6 – 7**, suggest replacing **the gamma reference voltage** with **the gamma reference voltage corresponding to the one of the three primary colors**;

Appropriate correction is required.

Claim Rejections - 35 USC § 112

15. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the

art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

16. Claim 11 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventors, at the time the application was filed, had possession of the claimed invention.

Specifically, the limitation, ***a shift register receiving*** ***and outputting image data of the three primary colors in*** ***a sequence of the time slots*** ***within each of the scan durations of the horizontal lines****,* was not described in the original disclosure.

The originally-filed specification discloses that "*[the] shift register 8 receives and outputs image data of the three primary colors in a predetermined sequence of the primary colors within a scan duration of one of the horizontal lines*"; **original disclosure, page 8, lines 12 – 15.**

The definition of the "three time slots" is provided in reference to **Fig. 2** wherein the original specification discloses that "*each of the scan durations of the horizontal lines is divided into three time slots, R:ON, G:ON and B:ON. The switches Rsw, Gsw, and Bsw of the unit gain buffer 5a, 5b and 5c shown in FIG. 3 are closed (turned on) during the time slots R:ON, G:ON and B:ON for the image data of the three primary colors, red,*

green and blue, to be fed into the sub-pixels, respectively"; **original disclosure, page 5, lines 20 – 26.**

That is, the "three time slots" is defined with respect to the *output display timing* (or *output data line driving*). The "three time slots" is not defined with respect to the *writing of pixel data to the display driver* (i.e., the *reception of pixel data* by the display driver).

Claim Rejections - 35 USC § 102

17. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

18. Claims 11 – 13 and 14 are rejected under 35 U.S.C. 102(e) as being anticipated by **NOSE [US Patent Application 2002/0163490 A1]**.

As for claim 11, NOSE teaches a data driver of a display forming an image frame by sequentially scanning horizontal lines

[Fig. 1 illustrates an LCD display driver**]**,

wherein each of scan durations of the horizontal lines is divided into three time slots respectively corresponding to three primary colors

> **[Fig. 2** illustrates the horizontal scanning of image data corresponding to the primary colors, red, green and blue**]**,

the data driver comprising:

> **a shift register receiving and outputting image data of the three primary colors in a sequence of the time slots within each of the scan durations of the horizontal lines**
>
> **[Fig. 3** "shift register section" **63** and "data register section" **64** correspond to a "*shift register receiving and outputting image data*"; the "shift register section" aligns the incoming gray-scale data (D1, D2, or D3) into the "data register section".
>
> NOSE explains, "the gray-scale data being fed from the display control circuit 3, for example, *6 bits* of gray-scale data D1, D2, and D3 *are held in parallel* by the data register section 64 which is controlled by an output at each stage in a shift register section 63 that is controlled by a horizontal start pulse HSP and a clock signal HCK"; **page 6, paragraph 83, lines 4 – 9.**

NOSE further teaches, “The gray-scale data for the R color, gray-scale data for the G color, and gray-scale data for the B color, all being fed from the display control circuit 3, *are sequentially switched in a repeated manner in every scanning position, as shown in Fig. 2*. Moreover, in this example, gray-scale data D1, D2, and D3 are transferred to the data register section 64 of the signal line driving circuit 6 through three ports, as shown in Fig. 3”; **page 7, paragraph 83, lines 6 – 8.**

Fig. 2 illustrates a “scan duration of one horizontal line” consisting of red pixel data which is then followed, in sequence, by green pixel data, and then blue pixel data. In this example, this sequence is repeated until all 480 lines of a frame are displayed**];**

a sample and hold register acquiring the image data from the shift register [Fig. 3 “data register section” **64** and “latch section” **65** correspond to the “sample and hold register”.

As noted above, NOSE teaches, “the gray-scale data being fed from the display control circuit 3, for example, 6 bits of gray-scale data D1, D2, and D3 are held in parallel by the data register section 64 which is controlled by an output at each stage in a shift register section 63 that is controlled by a horizontal start pulse HSP and a clock signal HCK”; **page 6, paragraph 83, lines 4 – 9.**

NOSE further teaches, “The signals making up gray-scale data D1, D2, and D3 being held in parallel in the data register section 64 are collectively transferred by a latch signal STB to a latch section 65 and latched therein”; **page 6, paragraph 83, lines 9 - 12];**

a gamma multiplexer outputting gamma reference voltages for the three primary colors in the sequence of the time slots

[Fig. 3 “RGB switching reference gray-scale voltage producing circuit” **4** contains a multiplexer consisting of multiplexers **M1, M2, …, M10** which is controlled by a common signal **SL**.

NOSE cites,” voltages obtained by selecting from voltages V0R, V0G, V0B, …, V9R, V9G, and V9B which are obtained by dividing a reference voltage V_{REF} using a voltage dividing circuit for a R color (DR), a voltage dividing circuit for a G color (DG), and a voltage dividing circuit for a B color (DB), respectively, for every color of the R, G, and B colors in accordance with a selection control signal SL using MPXs (multiplexers) M1, M2, …, M9, and M10, are output, through voltage followers B1, B2, …, B9, and B10, as reference gray-scale voltages V0, V1, V1, …, V8, and V9”; **page 6, paragraph 82, lines 2 – 12.** “Each of the MPXs M1, M2, …, M9, and M10 selects a corresponding voltage in response to the selection control signal SL being output in synchronization with the selection

of the scanning line 21 for each of the R, G, and B colors and outputs it as the reference gray-scale voltage to the signal line driving circuit 6"; **page 6, paragraph 82, lines 15 – 20];**

a digital-to-analog converter for gamma calibration, receiving the image data from the sample and hold register and the gamma reference voltages from the gamma multiplexer, and outputting calibrated image signals of the three primary colors

[Fig. 3 "DAC" **62** is a digital-to-analog converter which receives the image data from the sample-and-hold register ("data register section" **64** and "latch section" **65**) after the data is passed through a "level shift section 66" [**page 6, paragraph 83, lines 14 – 15**]. The DAC reference voltage, for each of the three primary colors - red, green, and blue, is provided through multiplexer **61.** "Gray-scale data D1, D2, and D3 having been transferred to the DAC 62 undergo the gamma correction based on the set of the reference gray-scale voltages V0 to V4 and the set of the reference gray-scale voltages V5 to V9 fed from the MPX 61, and at the same time, causes a D/A converted signal voltage to be generated which is output through the voltage followers F1, F2, …, F639, and F640 to each of the corresponding signal lines 22"; **page 6, paragraph 83, line 15 – page 7, paragraph 83, line 6];**

and a buffer receiving the calibrated image signals from the digital-to-analog converter and outputting the calibrated image signals in the sequence of the time slots

[Fig. 3 “voltage followers” **F1, F2, …, F640** correspond to the “buffer receiving the calibrated image signals from the digital-to-analog converter”**].**

Regarding claim 12, NOSE further teaches the data driver of claim 11, wherein

the gamma multiplexer outputs

the gamma reference voltages for a first primary color of the three primary colors within the time slot corresponding to the first primary color

[Fig. 2 illustrates a time period during which the “reference gray-scale voltage” for the red pixels is selected (e.g., line with pixels R1.1, R1.2, R1.3, …)**],**

the gamma reference voltages for a second primary color of the three primary colors within the time slot corresponding to the second primary color

[Fig. 2 illustrates a time period during which the “reference gray-scale voltage” for the green pixels is selected (e.g., line with pixels G1.1, G1.2, G1.3, …)**];**

and the gamma reference voltages for a third primary color of the three primary colors within the time slot corresponding to the third primary color

[Fig. 2 illustrates a time period during which the “reference gray-scale voltage” for the blue pixels is selected (e.g., line with pixels B1.1, B1.2, B1.3, …)**],**

wherein the time slot corresponding to the second primary color is subsequent to the time slot corresponding to the first primary color and the time slot corresponding to the third primary color is subsequent to the time slot corresponding to the second primary color

[As shown in **Fig. 3**, the “time slots” are sequenced in the order – red, green, blue, red, green, blue, …**].**

<u>Regarding claim 13</u>, NOSE further teaches the data driver of claim 12, wherein

the shift register receives *[and]* outputs

the image data of the first primary color within the time slot corresponding to the first primary color,

the image data of the second primary color within the time slot corresponding to the second primary color,

and image data of the third primary color within the time slot corresponding to the third primary color

[These limitations are implied by the *driver configuration* shown in **Fig. 3** and the corresponding *display driving method* shown in **Fig. 2** since the *driver*

configuration has a width of 640 pixels (i.e., the number of pixels in one horizontal scanning line) and the *display driving method* outputs one line (i.e., 640 pixels) of red, followed by one line of green, then one line of blue and so on**]**.

As for claim 14, NOSE teaches a method for driving a display forming an image frame by sequentially scanning horizontal lines

[Fig. 1 illustrates an LCD display driver**]**,

wherein each of scan durations of the horizontal lines is divided into three time slots respectively corresponding to three primary colors

[Fig. 2 illustrates the horizontal scanning of image data corresponding to the primary colors, red, green and blue**]**,

the method comprising:

receiving image data of the three primary colors within each of the scan durations of the horizontal lines

[As noted for claim 11, **Fig. 3** "shift register section" **63** and "data register section" *receive image data of one of the three primary colors within each of the scan durations of the horizontal lines***];**

generating gamma reference voltages for the three primary colors in a sequence of the time slots within each of the scan durations of the horizontal lines

[As noted for claim 11, **Fig. 3** "RGB switching reference gray-scale voltage producing circuit" **4** *generates a gamma reference voltage for the three primary colors in a sequence of the time slots within each of the scan durations of the horizontal lines***];**

and generating calibrated image signals of the three primary colors according to the image data of the three primary colors and the reference voltages in the sequence of the time slots

[As noted for claim 11, **Fig. 3** "DAC" **62** *generates calibrated image signals of the three primary colors according to the image data and the reference voltages in the sequence of the time slots***].**

Claim Rejections - 35 USC § 103

19. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

20. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

21. Claims 2, 5 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over **NOSE [US Patent Application 2002/0163490 A1]** in view of **HASHIMOTO [US Patent 6,181,311 B1]**.

<u>As for claim 2</u>, NOSE teaches a data driver of a display

[Fig. 1 illustrates an LCD display driver**]**

forming an image frame <u>divided into three sub-frames respectively corresponding to three primary colors</u>

by sequentially scanning horizontal lines

[Fig. 2 illustrates the horizontal scanning of image data corresponding to the primary colors, red, green and blue**]**,

the data driver comprising:

~~a shift register receiving image data of three primary colors in serial and~~ ~~*outputting the image data of the three primary colors in parallel*~~ ~~within each of scan durations of the horizontal lines~~

<u>a shift register receiving and outputting image data of one of the three primary colors *within the sub-frame corresponding to the one of the three primary colors*</u>

[Fig. 3 "shift register section" **63** and "data register section" **64** correspond to a "*shift register receiving and outputting image data*"; the "shift register section" aligns the incoming gray-scale data (D1, D2, or D3) into the "data register section".

NOSE explains, "the gray-scale data being fed from the display control circuit 3, for example, *<u>6 bits</u>* of gray-scale data D1, D2, and D3 *<u>are held in parallel</u>* by the data register section 64 which is controlled by an output at each stage in a shift register section 63 that is controlled by a horizontal start pulse HSP and a clock signal HCK"; **page 6, paragraph 83, lines 4 – 9.**

NOSE further teaches, "The gray-scale data for the R color, gray-scale data for the G color, and gray-scale data for the B color, all being fed from the display control circuit 3, *<u>are sequentially switched in a repeated manner in every scanning position, as shown in Fig. 2</u>*. Moreover, in this example, gray-scale data D1, D2, and D3 are transferred to the data register section 64 of the signal

line driving circuit 6 through three ports, as shown in Fig. 3"; **page 7, paragraph 83, lines 6 – 8.**

Fig. 2 illustrates a "scan duration of one horizontal line" consisting of red pixel data which is then followed, in sequence, by green pixel data, and then blue pixel data. In this example, this sequence is repeated until all 480 lines of a frame are displayed**];**

a sample and hold register acquiring the image data of <u>the one of</u> the three primary colors from the shift register

[Fig. 3 "data register section" **64** and "latch section" **65** correspond to the "sample and hold register";

As noted above, NOSE teaches, "the gray-scale data being fed from the display control circuit 3, for example, 6 bits of gray-scale data D1, D2, and D3 are held in parallel by the data register section 64 which is controlled by an output at each stage in a shift register section 63 that is controlled by a horizontal start pulse HSP and a clock signal HCK"; **page 6, paragraph 83, lines 4 – 9.**

NOSE further teaches, "The signals making up gray-scale data D1, D2, and D3 being held in parallel in the data register section 64 are collectively transferred by

a latch signal STB to a latch section 65 and latched therein"; **page 6, paragraph 83, lines 9 - 12];**

~~**a first multiplexer receiving the image data of the three primary colors from the sample and hold register and outputting them in a sequence of the primary colors within each of the scan durations of the horizontal lines;**~~

~~**a second multiplexer outputting gamma reference voltages for the three primary colors in the sequence of the primary colors within each of the scan durations of the horizontal lines;**~~

a gamma multiplexer outputting a gamma reference voltage corresponding to the one of the three primary colors *within the sub-frame corresponding to the one of the three primary colors*

[Fig. 3 "RGB switching reference gray-scale voltage producing circuit" **4** contains a multiplexer consisting of multiplexers **M1, M2, …, M10** which is controlled by a common signal **SL**.

NOSE cites," voltages obtained by selecting from voltages V0R, V0G, V0B, …, V9R, V9G, and V9B which are obtained by dividing a reference voltage V_{REF} using a voltage dividing circuit for a R color (DR), a voltage dividing circuit for a G color (DG), and a voltage dividing circuit for a B color (DB), respectively, for

every color of the R, G, and B colors in accordance with a selection control signal SL using MPXs (multiplexers) M1, M2, ..., M9, and M10, are output, through voltage followers B1, B2, ..., B9, and B10, as reference gray-scale voltages V0, V1, V1, ..., V8, and V9"; **page 6, paragraph 82, lines 2 – 12.** "Each of the MPXs M1, M2, ..., M9, and M10 selects a corresponding voltage in response to the selection control signal SL being output in synchronization with the selection of the scanning line 21 for each of the R, G, and B colors and outputs it as the reference gray-scale voltage to the signal line driving circuit 6"; **page 6, paragraph 82, lines 15 – 20];**

a digital-to-analog converter for gamma calibration, receiving the image data from the ~~first multiplexer~~ sample and hold register and the gamma reference voltage ~~voltages~~ from the ~~second~~ gamma multiplexer, and outputting a calibrated image signal ~~signals of the three primary colors~~

[Fig. 3 "DAC" **62** is a digital-to-analog converter which receives the image data from the sample-and-hold register ("data register section" **64** and "latch section" **65**) after the data is passed through a "level shift section 66" [**page 6, paragraph 83, lines 14 – 15**]. The DAC reference voltage, for each of the three primary colors - red, green, and blue, is provided through multiplexer **61.** "Gray-scale data D1, D2, and D3 having been transferred to the DAC 62 undergo the gamma correction based on the set of the reference gray-scale voltages V0 to V4 and the set of the reference gray-scale voltages V5 to V9 fed from the MPX 61, and at

the same time, causes a D/A converted signal voltage to be generated which is output through the voltage followers F1, F2, …, F639, and F640 to each of the corresponding signal lines 22"; **page 6, paragraph 83, line 15 – page 7, paragraph 83, line 6];**

and a buffer receiving the calibrated image <u>signal</u> ~~signals~~ from the digital-to- analog converter ~~and outputting the calibrated image signals in the sequence of the primary colors~~

[Fig. 3 "voltage followers" **F1, F2, …, F640** correspond to the "buffer receiving the calibrated image signals from the digital-to-analog converter"**]<u>,</u>**

<u>wherein the horizontal lines are sequentially scanned within each of the sub-frames</u>.

However, NOSE does not teach

forming an image frame <u>divided into three sub-frames respectively corresponding to three primary colors</u>,

<u>wherein the horizontal lines are sequentially scanned within each of the sub-frames</u>.

Therefore, NOSE also does not teach

a shift register receiving and outputting image data of one of the three primary colors *within the sub-frame corresponding to the one of the three primary colors*

a gamma multiplexer outputting a gamma reference voltage corresponding to the one of the three primary colors *within the sub-frame corresponding to the one of the three primary colors*

With references to **Figs. 1** and **2**, HASHIMOTO teaches a *display driving method* in which primary color images are displayed in *successive sub-frames*. "In period **1F**, the symbol t_A denotes an R signal writing period; $t_{A'}$, an R displaying period; t_B, a G signal writing period; $t_{B'}$, a G displaying period; t_C, a B signal writing period; and $t_{C'}$, a B displaying period"; **col. 5, lines 14 – 17.**

In this manner, "B, R, and G are successively displayed in period 1F, and the three colors are visually synthesized by afterimage effect to be recognized as a full color display"; **col. 5, lines 50 – 52.**

That is, HASHIMOTO teaches

forming an image frame divided into three sub-frames respectively corresponding to three primary colors

[“In period **1F**, the symbol t_A denotes an R signal writing period; $t_{A'}$, an R displaying period; t_B, a G signal writing period; $t_{B'}$, a G displaying period; t_C, a B signal writing period; and $t_{C'}$, a B displaying period”; **col. 5, lines 14 – 17],**

<u>wherein the horizontal lines are sequentially scanned within each of the sub-frames</u>

[Note the timing of signals $\mathbf{H_{11}}$, $\mathbf{H_{12}}$ and $\mathbf{H_{13}}$ in each of $\mathbf{V_1}$, $\mathbf{V_2}$, and $\mathbf{V_3}$ of **Fig. 2**; that is, $\mathbf{V_1}(\mathbf{H_{11}}, \mathbf{H_{12}}, \mathbf{H_{13}})$, $\mathbf{V_2}(\mathbf{H_{11}}, \mathbf{H_{12}}, \mathbf{H_{13}})$, and $\mathbf{V_3}(\mathbf{H_{11}}, \mathbf{H_{12}}, \mathbf{H_{13}})$**].**

The RGB data sequencing occurs by “selectively *switching*” red, green, and blue data to be sent to the display panel of **Fig. 1**. With reference to **Fig. 3**, the “external signal treatment memory” **33** converts the “signals from signal source 32 to drive signals to be transmitted to display panel 31, and outputs plane-sequentially as R, G, and B signals”; **col. 6, lines 7 – 10.**

That is, the *display driving method* is achieved by the “external signal treatment memory” **33** which is *<u>external</u>* to the “display panel”. The “external signal treatment memory” **33** *<u>sorts the RGB gray-scale data</u> which is then sent to the display panel.*

NOSE similarly teaches “<u>sorting</u>” the RGB gray-scale data which is then sent to the display panel. “The sorting of gray-scale data in the display control circuit 3 is performed in a way as shown in FIG. 2. FIG. 2 shows *<u>an example in the case of a</u>*

video graphics array (VGA) (640 x RGB x 480 pixels)"; **page 6, paragraph 80, lines 1 – 4.**

In this example, the *display driver configuration* of **Fig. 3** is driven in *a (horizontal) scanning line sequential manner* as shown in **Fig. 2.** That is, NOSE teaches

> *a shift register that receives and outputs image data of one of the three primary colors within a (horizontal) scanning line corresponding to one of the three primary colors,*
>
> and a *gamma multiplexer that outputs a gamma reference voltage corresponding to the one of the three primary colors within the (horizontal) scanning line corresponding to the one of the three primary colors.*

Since both types of *display driving methods* (i.e., *scanning line sequential* and *sub-frame sequential*) were known at the time the instant invention was made, it is believed that it would have been obvious to one of ordinary skill in the art at the time the invention was made to alternatively drive NOSE's *display driver configuration* of **Fig. 3** in the sub-frame sequential *manner* as taught by HASHIMOTO by changing the "*external sorting means*".

If RGB gray-scale data were to be externally sorted into *sub-frames of red, green, and blue data*, as taught by HASHIMOTO, NOSE's "shift register" of **Fig. 3** would then

receive and output image data of one of the three primary colors within a sub-frame corresponding to one of the three primary colors.

In this case, it would have been obvious to additionally alter the *selection timing* of NOSE's "gamma multiplexer" (of **Fig. 3**) to *output a gamma reference voltage corresponding to the one of the three primary colors within the sub-frame corresponding to the one of the three primary colors.* That is, it would have been obvious to change the gamma reference voltage *for each sub-frame* instead of *for each scanning line*.

Regarding claim 5, NOSE *does not specifically teach* the data driver of claim 2, wherein

> **the image frame comprises a first sub-frame corresponding to a first primary color of the three primary colors,**
>
> **a second sub-frame corresponding to a second primary color of the three primary colors,**
>
> **and a third sub-frame corresponding to a third primary color of the three primary colors,**
>
> **wherein the second sub-frame is subsequent to the first sub-frame and the third sub-frame is subsequent to the second sub-frame.**

However, HASHIMOTO's *display driving method* teaches these limitations; specifically,

the image frame comprises a first sub-frame corresponding to a first primary color of the three primary colors

[With reference to **Fig. 2**, the first sub-frame corresponds to the color red, t_A and $t_{A'}$.**],**

a second sub-frame corresponding to a second primary color of the three primary colors

[With reference to **Fig. 2**, the second sub-frame corresponds to the color green, t_B and $t_{B'}$.**],**

and a third sub-frame corresponding to a third primary color of the three primary colors

[With reference to **Fig. 2**, the third sub-frame corresponds to the color blue, t_C and $t_{C'}$.**],**

wherein the second sub-frame is subsequent to the first sub-frame and the third sub-frame is subsequent to the second sub-frame

[This sequence is shown in **Fig. 2].**

As for claim 15, NOSE teaches a method for driving a display forming an image frame *divided into three sub-frames respectively corresponding to three primary colors*

by sequentially scanning horizontal lines

[Fig. 2 illustrates the horizontal scanning of image data corresponding to the primary colors, red, green and blue**]**,

the method comprising:

receiving image data of one of the three primary colors *within the sub-frame corresponding to the one of the three primary colors*

[As noted for claim 1, **Fig. 3** “shift register section” **63** and “data register section” **64** *receive image data of one of the three primary colors <u>within a (horizontal) scanning line</u> corresponding to the one of the three primary colors.*

However, NOSE *does not specifically* teach sorting the RGB gray-scale data into *sub-frames.***];**

generating a gamma reference voltage corresponding to the one of the three primary colors *within the sub-frame corresponding to the one of the three primary colors*

[As noted for claim 1, **Fig. 3** “RGB switching reference gray-scale voltage producing circuit” **4** *generates a gamma reference voltage corresponding to the one of the three primary colors <u>within the (horizontal) scanning line</u> corresponding to the one of the three primary colors.*

However, NOSE *does not specifically* teach sorting the RGB gray-scale data into *sub-frames.*];

and generating a calibrated image signal according to the image data and the gamma reference voltage

[As noted for claim 1, **Fig. 3** "DAC" **62** *generates a calibrated image signal according to the image data and the gamma reference voltage***],**

wherein the horizontal lines are sequentially scanned *within each of the sub-frames*

[As noted for claim 1, ***Fig. 2*** *illustrates a "scan duration of one horizontal line" consisting of red pixel data which is then followed, in sequence, by green pixel data, and then blue pixel data. This sequence is repeated until all 480 lines of a frame are displayed.*

However, NOSE *does not specifically* teach sorting the RGB gray-scale data into *sub-frames.*].

As noted for claim 1, HASHIMOTO teaches a *display driving method* in which primary color images are displayed in *successive sub-frames*, and *wherein the horizontal lines are sequentially scanned within each of the sub-frames.*

HASHIMOTO's "external signal treatment memory" **33** (of **Fig. 3**) _sorts the RGB gray-scale data_ *which is then sent to the display panel.*

Also noted for claim 1, since both types of _display driving methods_ (i.e., *scanning line sequential* and *sub-frame sequential*) were known at the time the instant invention was made, it is believed that it would have been obvious to one of ordinary skill in the art at the time the invention was made to alternatively drive NOSE's *display driver configuration* of **Fig. 3** in the sub-frame sequential *manner* as taught by HASHIMOTO by changing the "*external sorting means*".

If RGB gray-scale data were to be externally sorted into *sub-frames of red, green, and blue data*, as taught by HASHIMOTO, NOSE's "shift register" of **Fig. 3** would then *receive and output image data of one of the three primary colors within* _a sub-frame_ *corresponding to one of the three primary colors*.

In this case, it would have been obvious to additionally alter the *selection timing* of NOSE's "gamma multiplexer" (of **Fig. 3**) to *output a gamma reference voltage corresponding to the one of the three primary colors within* _the sub-frame_ *corresponding to the one of the three primary colors.* That is, it would have been obvious to change the gamma reference voltage _for each sub-frame_ (primary color) instead of _for each scanning line_ (primary color).

22. Claims 6 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over **NOSE [US Patent Application 2002/0163490 A1]**.

As for claim 6, NOSE teaches a data driver of a display forming an image frame by sequentially scanning horizontal lines

[Fig. 10 illustrates an LCD display driver**]**,

wherein each of scan durations of the horizontal lines is divided into three time slots respectively corresponding to three primary colors,

the data driver comprising:

a shift register receiving image data of the three primary colors in serial and outputting the image data of the three primary colors in parallel within each of the scan durations of the horizontal lines

[Fig. 11 "shift register section" **163** and "data register section" **164** hold image data for red, green and blue channels *simultaneously*;

NOSE cites, "6 bits of R-color gray-scale data DR, 6 bits of G-color gray-scale data DG, and 6 bits of B-color gray-scale data DB all being fed from the display control circuit 13 are held, in parallel, in a data register section 164 being controlled by an output, which is controlled by a horizontal start pulse HSP and a

clock signal HCK, fed at each stage in a shift register section 163” **page 2, paragraph 12, lines 1 - 7];**

a sample and hold register acquiring the image data from the shift register [Fig. 11 “data register section” **164** and “latch section” **165** correspond to the “sample and hold register”;

NOSE teaches, “The … gray-scale data DR, DG, and DB” (which are not the same as DR, DG and DB shown in Fig. 3) “being held in parallel in the data register section 164 are transferred collectively to a latch section 165 by a latch signal STB and then are latched therein”; **page 2, paragraph 12, lines 7 – 11];**

a gamma multiplexer outputting gamma reference voltages for the three primary colors in a sequence of the time slots within each of the scan durations of the horizontal lines;

three digital-to-analog converters for gamma calibration, receiving the image data of the three primary colors from the sample and hold register [Fig. 11 “DAC” **162** is a digital-to-analog converter which receives the image data from the sample-and-hold register (“data register section” **164** and “latch section” **165**) after the data is passed through a “level shift section 166” [**page 2, paragraph 12, lines 12 – 13**].

Note that for each pixel, there are *three digital-to-analog converters* – one for each of the red, green and blue color channels**]**

and the gamma reference voltages for the three primary colors from the gamma multiplexer, and outputting calibrated image signals of the three primary colors, respectively;

and three buffers respectively receiving the calibrated image signals of the three primary colors from the three digital-to-analog converters, in the sequence of the time slots

[Fig. 11 “voltage followers” **F1, F2, …, F1920** are the separate buffers for each color (red, green, blue) pixel (in a horizontal scan). NOSE cites, “Fig. 11 shows an example in which voltages corresponding to the gray-scale data are output to 1920 pieces of the pixel electrodes 123 corresponding to 640 pieces of color pixels arranged in a horizontal direction in a liquid crystal panel 12”; **page 2, paragraph 11, lines 3 – 7.**

Although shown as 1920 separate buffers (one for each color pixel), partitioning these 1920 separate buffers as three groups of buffers, one for each primary color, is equivalent**].**

However, with respect to this *prior art embodiment*, NOSE *does not specifically teach*

each of the scan durations of the horizontal lines is divided into three time slots respectively corresponding to three primary colors

a gamma multiplexer outputting gamma reference voltages for the three primary colors in a sequence of the time slots within each of the scan durations of the horizontal lines;

and *supplying*

the gamma reference voltages for the three primary colors *[to the three digital-to-analog converters]* ***from the gamma multiplexer, and outputting calibrated image signals of the three primary colors, respectively;***

However, as shown in **Fig. 3**, NOSE teaches a

a gamma multiplexer outputting gamma reference voltages for the three primary colors in a sequence of the time slots within each of the scan durations of the horizontal lines;

Fig. 3 “RGB switching reference gray-scale voltage producing circuit” **4** contains a multiplexer consisting of multiplexers **M1, M2, …, M10** which is controlled by a common signal **SL**;

NOSE cites," voltages obtained by selecting from voltages V0R, V0G, V0B, …, V9R, V9G, and V9B which are obtained by dividing a reference voltage V_{REF} using a voltage dividing circuit for a R color (DR), a voltage dividing circuit for a G color (DG), and a voltage dividing circuit for a B color (DB), respectively, for every color of the R, G, and B colors in accordance with a selection control signal SL using MPXs (multiplexers) M1, M2, …, M9, and M10, are output, through voltage followers B1, B2, …, B9, and B10, as reference gray-scale voltages V0, V1, V1, …, V8, and V9"; **page 6, paragraph 82, lines 2 – 12.** "Each of the MPXs M1, M2, …, M9, and M10 selects a corresponding voltage in response to the selection control signal SL being output in synchronization with the selection of the scanning line 21 for each of the R, G, and B colors and outputs it as the reference gray-scale voltage to the signal line driving circuit 6"; **page 6, paragraph 82, lines 15 – 20.**

It would have been obvious to one of ordinary skill in the art at the time the invention was made to add NOSE's teachings of a "***gamma multiplexer***" (or "RGB switching reference gray-scale voltage producing circuit") with the *prior art* as taught by NOSE to improve image quality.

With the *substitution* of the "RGB switching reference gray-scale voltage producing circuit", shown in **Fig. 3** as reference number **4**, in place of the "reference gray-scale voltage producing circuit", shown in **Fig. 11** as reference number **14**, it would have been obvious to one of ordinary skill in the art at the time the invention was made to ***supply***

the three digital-to-analog converters with <u>gamma reference voltages for the three primary colors from the gamma multiplexer</u> so as to produce ***calibrated image signals of the three primary colors***.

In this case, it would have also been obvious to additionally *synchronize and "gate" the outputs of the digital-to-analog converters with the timing of the gamma reference voltages* so that a converted analog voltage for a primary color pixel correctly reflects the supplied *gamma reference voltage*.

When the outputs of the digital-to-analog converters are synchronized and "gated" in this manner, *each of the scan durations of the horizontal lines is divided into three time slots respectively corresponding to three primary colors.*

<u>Regarding claim 7</u>, NOSE further teaches the data driver of claim 6, wherein

> **the gamma multiplexer outputs**
>
> **the gamma reference voltages for a first primary color of the three primary colors within the time slot corresponding to the first primary color**
>
> **[Fig. 2** illustrates a time period during which the "reference gray-scale voltage" for the red pixels is selected (e.g., line with pixels R1.1, R1.2, R1.3, …)**],**

the gamma reference voltages for a second primary color of the three primary colors within the time slot corresponding to the second primary color

[Fig. 2 illustrates a time period during which the "reference gray-scale voltage" for the green pixels is selected (e.g., line with pixels G1.1, G1.2, G1.3, …)**],**

and the gamma reference voltages for a third primary color of the three primary colors within the time slot corresponding to the third primary color

[Fig. 2 illustrates a time period during which the "reference gray-scale voltage" for the blue pixels is selected (e.g., line with pixels B1.1, B1.2, B1.3, …)**],**

wherein the time slot corresponding to the second primary color is subsequent to the time slot corresponding to the first primary color and the time slot corresponding to the third primary color is subsequent to the time slot corresponding to the second primary color

[As shown in **Fig. 3**, the "time slots" are sequenced in the order – red, green, blue, red, green, blue, …**].**

23. Claims 8 – 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over **NOSE [US Patent Application 2002/0163490 A1]** in view of **LEE [US Patent Application 2003/0132907 A1]** and in view of *prior art* as taught by NOSE.

<u>As for claim 8</u>, NOSE teaches a data driver of a display forming an image frame by sequentially scanning horizontal lines

[Fig. 10 illustrates an LCD display driver**]**,

wherein each of scan durations of the horizontal lines is divided into three time slots respectively corresponding to three primary colors,

the data driver comprising:

a shift register receiving image data of three primary colors in serial and outputting the image data of the three primary colors in parallel within each of the scan durations of the horizontal lines

[Fig. 11 “shift register section” **163** and “data register section” **164** hold image data for red, green and blue channels *simultaneously*;

NOSE cites, “6 bits of R-color gray-scale data DR, 6 bits of G-color gray-scale data DG, and 6 bits of B-color gray-scale data DB all being fed from the display control circuit 13 are held, in parallel, in a data register section 164 being controlled by an output, which is controlled by a horizontal start pulse HSP and a clock signal HCK, fed at each stage in a shift register section 163” **page 2, paragraph 12, lines 1 - 7];**

a sample and hold register acquiring the image data of the three primary colors from the shift register

[Fig. 11 “data register section” **164** and “latch section” **165** correspond to the “sample and hold register”;

NOSE teaches, “The … gray-scale data DR, DG, and DB” (which are not the same as DR, DG and DB shown in Fig. 3) “being held in parallel in the data register section 164 are transferred collectively to a latch section 165 by a latch signal STB and then are latched therein”; **page 2, paragraph 12, lines 7 – 11];**

a first multiplexer receiving the image data of the three primary colors from the sample and hold register and outputting them in a sequence of the time slots within each of the scan durations of the horizontal lines;

a second multiplexer outputting gamma reference voltages for the three primary colors in the sequence of the time slots within each of the scan durations of the horizontal lines;

a digital-to-analog converter for gamma calibration, receiving the image data from the first multiplexer and the gamma reference voltages from the second multiplexer, and outputting calibrated image signals of the three primary colors;

and a buffer receiving the calibrated image signals from the digital-to-analog converter and outputting the calibrated image signals in the sequence of the time slots

[Fig. 11 “voltage followers” **F1, F2, F3, …, F1920].**

However, with respect to this *prior art embodiment*, NOSE *does not specifically teach*

[1] *each of scan durations of the horizontal lines is divided into three time slots respectively corresponding to three primary colors*

[2] ***a first multiplexer receiving the image data of the three primary colors from the sample and hold register and outputting them in a sequence of the time slots within each of the scan durations of the horizontal lines;***

[3] ***a second multiplexer outputting gamma reference voltages for the three primary colors in the sequence of the time slots within each of the scan durations of the horizontal lines;***

and **[4]** supplying ***the gamma reference voltages*** *[to the digital-to-analog converter]* ***from the second multiplexer, and outputting calibrated image signals of the three primary colors;***

Regarding limitation **[2]**, LEE's invention "provides an apparatus and method for driving a liquid crystal display wherein a digital to analog converter part is driven on a time-division basis to increase the number of output channels of the data driving IC while the chip area is not greatly increased or reduced in comparison to the existing chip area, thereby reducing the number of data driving IC's and TCP's"; **page 2, paragraph 23, lines 1 – 8.**

With reference to **Figs. 4 - 6**, LEE teaches

a first multiplexer receiving the image data of the three primary colors from the sample and hold register

[Figs. 4, 5 "latch part" **36** which is controlled by the "shift register part" **34** and **Fig. 6** "latch" **46** correspond to the "sample and hold register"; **Figs. 4, 5** "mux part" **38** and **Fig. 6** "multiplexor" **48** corresponds to the "first multiplexor".

"FIG. 6 illustrates a transmission path of three red (R), green (G), and blue (B) pixel data within the data driving IC shown in FIG. 5"; **page 4, paragraph 57, lines 1 – 3]**

and outputting them in a sequence of the time slots within each of the scan durations of the horizontal lines

> **[**"The multiplexor 48 performs a time-division of the R, G, and B pixel data inputted from the three latches 46 to sequentially supply the time-divided pixel data to a single DAC 50"; **page 4, paragraph 59, lines 1 – 4.**
>
> In this manner, "in the data driving IC ..., the number of DAC's are reduced to at least 1/3 by a time-divisional driving of the DAC part, thereby reducing a space occupied by the DAC part within the IC"; **page 5, paragraph 67, lines 1 - 5];**

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of LEE with those of NOSE by adding a "***<u>first multiplexer receiving the image data of the three primary colors</u>***" from the sample and hold register as this would reduce the number of "digital-to-analog" and "buffer" functional blocks resulting in lower hardware cost.

Regarding limitations **[3]** and **[4]**, according to NOSE's first embodiment shown in **Fig. 3**, NOSE teaches

> ***a second multiplexer outputting gamma reference voltages for the three primary colors in the sequence of the time slots within each of the scan durations of the horizontal lines;***

Fig. 3 "RGB switching reference gray-scale voltage producing circuit" **4** contains a multiplexer consisting of multiplexers **M1, M2, …, M10** which is controlled by a common signal **SL**.

NOSE cites," voltages obtained by selecting from voltages V0R, V0G, V0B, …, V9R, V9G, and V9B which are obtained by dividing a reference voltage V_{REF} using a voltage dividing circuit for a R color (DR), a voltage dividing circuit for a G color (DG), and a voltage dividing circuit for a B color (DB), respectively, for every color of the R, G, and B colors in accordance with a selection control signal SL using MPXs (multiplexers) M1, M2, …, M9, and M10, are output, through voltage followers B1, B2, …, B9, and B10, as reference gray-scale voltages V0, V1, V1, …, V8, and V9"; **page 6, paragraph 82, lines 2 – 12.** "Each of the MPXs M1, M2, …, M9, and M10 selects a corresponding voltage in response to the selection control signal SL being output in synchronization with the selection of the scanning line 21 for each of the R, G, and B colors and outputs it as the reference gray-scale voltage to the signal line driving circuit 6"; **page 6, paragraph 82, lines 15 – 20.**

It would have been obvious to one of ordinary skill in the art at the time the invention was made to <u>add</u> NOSE's teachings of a "***<u>gamma multiplexer</u>***" (or "RGB switching reference gray-scale voltage producing circuit") with the *prior art* as taught by NOSE to improve image quality.

With the *substitution* of the “RGB switching reference gray-scale voltage producing circuit”, shown in **Fig. 3** as reference number **4**, in place of the “reference gray-scale voltage producing circuit”, shown in **Fig. 11** as reference number **14**, it would have been obvious to one of ordinary skill in the art at the time the invention was made to ***supply the digital-to-analog converter with <u>gamma reference voltages for the three primary colors from the gamma</u>*** <u>**(or second)**</u> ***<u>multiplexer</u>*** so as to produce ***calibrated image signals of the three primary colors***.

In this case, it would have also been obvious to additionally *synchronize and “gate” the outputs of the digital-to-analog converter with the timing of the gamma reference voltages* so that a converted analog voltage for a primary color pixel correctly reflects the supplied *gamma reference voltage*.

When the outputs of the digital-to-analog converters are synchronized and “gated” in this manner, *each of the scan durations of the horizontal lines is divided into three time slots respectively corresponding to three primary colors* (**limitation [1]**).

<u>Regarding claim 9</u>, NOSE further teaches the data driver of claim 8, wherein

> **the second multiplexer outputs**
>
> **the gamma reference voltages for a first primary color of the three primary colors within the time slot corresponding to the first primary color**

[Fig. 2 illustrates a time period during which the “reference gray-scale voltage” for the red pixels is selected (e.g., line with pixels R1.1, R1.2, R1.3, …)**],**

the gamma reference voltages for a second primary color of the three primary colors within the time slot corresponding to the second primary color

[Fig. 2 illustrates a time period during which the “reference gray-scale voltage” for the green pixels is selected (e.g., line with pixels G1.1, G1.2, G1.3, …)**],**

and the gamma reference voltages for a third primary color of the three primary colors within the time slot corresponding to the third primary color

[Fig. 2 illustrates a time period during which the “reference gray-scale voltage” for the blue pixels is selected (e.g., line with pixels B1.1, B1.2, B1.3, …)**],**

wherein the time slot corresponding to the second primary color is subsequent to the time slot corresponding to the first primary color and the time slot corresponding to the third primary color is subsequent to the time slot corresponding to the second primary color

[As shown in **Fig. 3**, the “time slots” are sequenced in the order – red, green, blue, red, green, blue, …**].**

<u>Regarding claim 10</u>, NOSE *does not specifically teach* the data driver of claim 9, wherein

> **the first multiplexer outputs the image data of the first primary color within the time slot corresponding to the first primary color,**
>
> **the image data of the second primary color within the time slot corresponding to the second primary color,**
>
> **and image data of the third primary color within the time slot corresponding to the third primary color**
> **[**As noted for claim 8, LEE's "multiplexor 48 performs a time-division of the R, G, and B pixel data inputted from the three latches 46 to sequentially supply the time-divided pixel data to a single DAC 50"; **page 4, paragraph 59, lines 1 – 4].**

Response to Arguments

24. Applicant's arguments filed **6/11/2009** have been fully considered but they are moot in view of the new grounds of rejection.

Conclusion

25. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Peter L. Cheng whose telephone number is 571-270-3007. The examiner can normally be reached on MONDAY - FRIDAY, 8:30 AM - 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, King Y. Poon can be reached on 571-272-7440. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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/plc/
September 25, 2009